Real-Time Logic Gate Recognition using Computer Vision

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Abstract

Hand-drawn digital logic gate recognition is a crucial advancement in the intersection of artificial intelligence and digital circuit design. This study presents an AI-powered system that enables real-time recognition and classification of hand-drawn logic gates using deep learning models. The primary objective is to bridge the gap between traditional circuit design methods and modern AI-assisted verification techniques, thereby streamlining learning, prototyping, and industrial applications. The proposed model leverages convolutional neural networks (CNNs) trained on an extensive dataset of manually drawn logic gates, including AND, OR, NOT, NAND, NOR, XOR, and XNOR. The system processes real-time input through a webcam interface, where pre- processing techniques such as skeletonization, edge detection, and contour analysis enhance the accuracy of classification. To further improve recognition, MobileNet SSD is utilized for object detection, ensuring robust and efficient performance. This research explores various application domains, including education, hardware prototyping, CAD tool integration, embedded systems, and industrial automation. In education, the system aids students in learning Boolean algebra and digital logic by providing instant feedback on hand-drawn circuits. Hardware designers benefit from quick logic gate validation before physical implementation, while AI-assisted CAD tools enable automatic sketch-to-schematic conversion. Moreover, real-time gate recognition can be integrated into edge computing devices for IoT-based logic circuit analysis, further enhancing its usability in research and industry. Experimental results demonstrate the model's effectiveness through multiple training scenarios, with varying levels of accuracy and loss convergence across different cases, including Case 4 and Case 5. The findings highlight the potential of AI-driven tools in automating circuit verification and accelerating the design process. Future enhancements will focus on expanding recognition to complex circuits, improving model generalization, and integrating it with FPGA and VLSI design workflows. This work underscores the transformative impact of AI in digital logic design, paving the way for more intelligent and interactive circuit development methodologies.

Keywords: *FPGA, Tkinter, MobileNet, XNOR Gate, VGG16, LTSpice.*

1. Introduction

Digital logic gates form the foundation of modern computing and electronic systems. These gates perform basic logical functions that are fundamental to digital circuits and are essential components in microprocessors, memory units, and control circuits. Traditionally, students and engineers design logic circuits using software tools

such as Logisim, LTSpice, and MATLAB, or by physically implementing them on breadboards. However, a significant challenge arises in the manual sketching and verification of logic gates, which can lead to misinterpretation and errors. The increasing reliance on artificial intelligence (AI) and machine learning (ML) for automation has led to the development of AI-powered tools that can recognize hand-drawn symbols and convert them into digital representations. This work aims to leverage deep learning models to develop an intelligent system capable of identifying and classifying hand- drawn logic gates. By integrating real-time detection, this system can serve as an automated learning aid for students, a debugging tool for engineers, and an industry solution for circuit verification.

Recognizing hand-drawn logic gates has several practical applications in education, industry, and research. In academic settings, students often sketch logic gates on paper or whiteboards to solve problems related to Boolean algebra and digital circuit design. The ability to automatically recognize and evaluate these sketches can significantly enhance the learning process, provide instant feedback and reduce manual evaluation efforts. For engineers and researchers, logic gate recognition plays a crucial role in early-stage circuit prototyping. Many preliminary designs are initially conceptualized as hand-drawn diagrams before being translated into digital schematics. Automating this process improves efficiency, reduces human error, and accelerates hardware implementation.

Additionally, in the semiconductor industry, logic gate recognition can be employed for quality control and automated testing. Recognizing hand-drawn circuits and converting them into structured schematics can streamline PCB design, ASIC development, and FPGA implementation, making circuit design more efficient and error-free.

Logic Gate Classification

Logic gates are classified based on their functionality and behavior in digital circuits. The fundamental logic gates include:

- **AND Gate**: Outputs high only when both inputs are high.
- **OR Gate**: Outputs high when at least one input is high.
- **NOT Gate (Inverter)**: Outputs the opposite logic state of the input.
- **NAND Gate**: Outputs the inverse of an AND gate.
- **NOR Gate**: Outputs the inverse of an OR gate.
- **XOR Gate**: Outputs high when the inputs are different.
- **XNOR Gate**: Outputs high when the inputs are the same.

Each of these gates has a distinct graphical representation, which makes their classification a fundamental challenge in AI-driven recognition systems. The complexity increases when dealing with hand-drawn variations due to inconsistencies in stroke patterns, sizes, and distortions.

Real-time detection of hand-drawn logic gates is a crucial feature that enhances user experience and applicability. A real-time system allows students to receive immediate feedback on their sketches, ensuring a dynamic and interactive learning process. This is particularly beneficial in remote learning environments where automated grading and feedback can support self-paced education. For engineers, real-time detection enables instant verification of circuit diagrams during brainstorming sessions or collaborative design processes. It also assists in on-the-fly corrections, preventing costly design errors before proceeding with hardware implementation.

In industrial applications, integrating real-time logic gate recognition with smart manufacturing systems can help in automated quality control and reduce the need for

manual inspections. The ability to scan and validate logic circuits in real time ensures that errors are caught early, leading to more reliable digital system designs.

The current methods of logic gate recognition largely depend on manual verification, which is both time-consuming and prone to human errors. Existing digital logic design tools do not provide real-time recognition and validation of hand-drawn circuits, thereby limiting their effectiveness in educational environments and early-stage prototyping. Furthermore, there is a lack of efficient systems to bridge the gap between hand-drawn circuit diagrams and their direct implementation in CAD tools. As a result, engineers and students often face difficulties in verifying logic circuits during the initial design stages, which can lead to errors in hardware implementation. Additionally, the absence of automated circuit evaluation methods in academic settings makes the assessment process inefficient and less effective in measuring students' understanding.

The objectives of this work are

- Develop an AI-powered system capable of recognizing and classifying hand-drawn digital logic gates in real time.
- Enhance accuracy and robustness of logic gate detection using machine learning and image processing techniques.

The motivation behind this work stems from the growing need for automation and accuracy in digital circuit design. Current approaches to logic gate recognition rely heavily on manual evaluation, which is time-consuming and prone to errors. By implementing a machine-learning based recognition system, we aim to address the following key challenges:

Enhancing Educational Tools: Providing students with an AI-driven platform that can automatically recognize and verify their hand-drawn logic circuits, making learning more interactive and efficient.

Reducing Human Error in Circuit Design: Automating logic gate recognition minimizes the risk of misinterpretation and incorrect circuit implementations.

Speeding up Circuit Prototyping: Engineers and designers can quickly validate hand-drawn circuits before moving to software simulation or hardware implementation.

Advancing AI Applications in Electronics: Integrating deep learning with digital logic design paves the way for future innovations in AI-assisted circuit design and verification.

By addressing these challenges, this work seeks to bridge the gap between traditional circuit design methods and modern AI-driven automation, ultimately improving efficiency, accuracy, and accessibility in digital logic design.

2. Literature Survey

Yann LeCun et al. (1998) introduced Convolutional Neural Networks (CNNs) for handwritten digit recognition. Their work demonstrated how spatial hierarchies of features can be automatically learned, forming the basis for recognizing hand-drawn logic gates. The LeNet architecture proved that CNNs outperform traditional pattern recognition techniques in accuracy and robustness. Alex Krizhevsky et al. (2012) proposed AlexNet, which revolutionized image classification. This work showed the power of deep CNNs with ReLU and dropout, enabling high-performance classification of complex visual patterns such as irregular hand-drawn gates. Visual Geometry Group (2014) introduced VGG16, a deep CNN architecture with small convolution filters. It provides high feature extraction capability, making it suitable for detecting subtle variations in hand-drawn logic gate shapes. Kaiming He et al. (2015) proposed ResNet, which uses skip connections to

overcome vanishing gradient problems. This enables training deeper models for improved classification accuracy in complex symbol datasets.

Google (2017) introduced MobileNet, optimized for edge devices. Its lightweight architecture is ideal for real-time logic gate recognition systems deployed on IoT devices. Wei Liu et al. (2016) proposed SSD, a real-time object detection framework. This method allows detection and classification of multiple logic gates simultaneously in live video streams. Joseph Redmon et al. (2016) introduced YOLO, which processes images in a single pass for extremely fast detection. It is highly relevant for real-time logic gate recognition. Davis et al. (2017) explored deep neural networks for sketch recognition, showing that models trained on sketch datasets can generalize well to hand-drawn diagrams, including logic circuits. Stankiewicz et al. (2018) proposed a system for recognizing hand-drawn electrical circuits using image processing and ML. Their work highlights challenges like noise, distortion, and symbol variability.

Dosch et al. (2000) developed techniques for symbol recognition in technical drawings, laying groundwork for modern AI-based circuit interpretation systems. Ahmed et al. (2019) introduced graph-based approaches to interpret circuit diagrams by converting symbols into structured representations, aiding CAD integration. Howard et al. (2019) extended MobileNet for real-time vision applications, demonstrating efficient deployment on low-power hardware. Holzinger et al. (2018) discussed AI in education, emphasizing automated feedback systems. This supports motivation of using logic gate recognition for student learning. Zhang et al. (2020) explored deep learning deployment on FPGA, showing how AI models can assist in hardware prototyping and verification. Kim et al. (2021) proposed systems integrating image recognition with CAD tools, enabling automatic conversion of sketches into digital schematics.

Dataset for Hand-Drawn Circuit Recognition (2025) introduces a large-scale dataset (JUHCCR-v1) specifically designed for hand-drawn electrical and electronic component recognition. It highlights the lack of benchmark datasets in this domain and provides annotated samples to improve model training. The dataset significantly contributes to improving deep learning-based recognition systems for logic gates and circuits. Agrawal et al. proposed a hybrid system combining machine learning and deep learning techniques for recognizing hand-drawn diagrams. The study demonstrates improved accuracy by integrating classical feature extraction with CNN-based models, especially for noisy sketches. Fuchs et al. developed a CNN + pattern matching approach for converting unstructured circuit diagrams into machine-readable formats. Their work emphasizes the importance of digitizing engineering drawings for maintenance and automation. Bohara and Krishnamoorthy proposed a YOLOv8-based detection system for identifying circuit components with high accuracy (~96.7% mAP). The framework integrates object detection with connectivity analysis for complete circuit understanding. Hemker et al. presented a system that converts circuit schematics into netlists using deep learning techniques. This enables automatic simulation and verification of circuits, bridging the gap between diagrams and implementation. Hu et al. proposed a Graph Attention Network (GAT) to extract circuit netlists from images. The method models relationships between components, enabling accurate interpretation of complex circuits.

The survey shows that deep learning techniques such as CNNs, YOLO, and graph-based models are highly effective for recognizing hand-drawn symbols and circuit diagrams. Earlier studies focus on image classification, while recent works emphasize real-time detection, improved datasets, and CAD integration. Overall, the research highlights a shift toward AI-based automation for accurate and efficient circuit design and verification.

3. Methodology

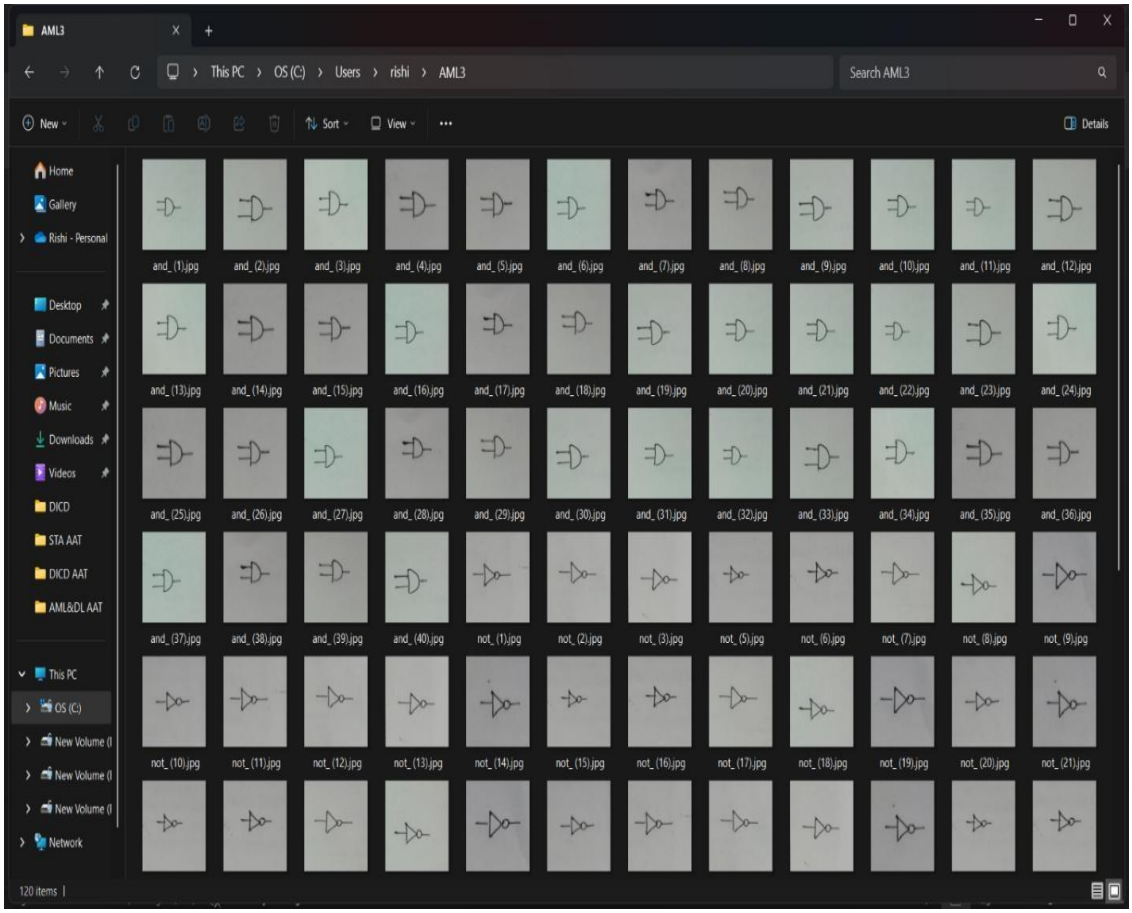


Figure 1: Dataset

Dataset Collection and Preprocessing

To develop an accurate logic gate recognition system, a robust dataset of hand-drawn logic gates is essential. The methodology involves:

Dataset Acquisition:

- Collecting hand-drawn logic gate images from various sources, including publicly available datasets and manually drawn samples.
- Augmenting the dataset by applying transformations such as rotation, scaling, noise addition, and contrast adjustments to improve model generalization.

Preprocessing Techniques:

- Converting images to grayscale to reduce computational complexity.
- Applying edge detection techniques (e.g., Canny edge detection, contour extraction) to enhance feature visibility.
- Using skeletonization to simplify hand-drawn structures for better classification.
- Resizing and normalizing images to ensure uniform input dimensions for the deep learning model

Model Selection and Training

Selecting an appropriate machine learning model is crucial for achieving high accuracy in logic gate classification. The methodology includes:

Model Architecture Selection:

- Experimenting with convolutional neural networks (CNNs) such as MobileNet, VGG16, and ResNet for efficient feature extraction.
- Fine-tuning a pre-trained MobileNet SSD model for real-time object detection of logic gates.

Training Process:

- Splitting the dataset into training, validation, and testing sets.
- Using cross-entropy loss as the objective function for classification.
- Employing data augmentation techniques during training to improve model robustness.
- Monitoring model performance using metrics such as accuracy, loss, precision, recall, and F1-score.
- Fine-tuning hyper parameters like learning rate, batch size, and dropout rate to optimize model performance.

Validation and Testing:

- Evaluating the trained model on unseen test data to assess generalization capability.
- Using confusion matrices and classification reports to analyze mis classifications

- Comparing different model architectures and selecting the best-performing one based on accuracy and computational efficiency.

Implementation Details

Once the model is trained, it is integrated into an interactive system that allows real-time logic gate recognition. The key implementation steps include:

User Interface Development:

- Implementing a graphical user interface (GUI) using Tkinter for easy user interaction.
- Providing options to upload images, draw logic gates on a digital canvas, or use a webcam for real-time detection.
- Displaying recognized logic gates and corresponding classification confidence.

Real-Time Detection Pipeline:

- Capturing real-time input through a webcam feed.
- Applying preprocessing techniques on each frame to enhance edge detection and contrast.
- Passing the processed image to the trained deep learning model for classification.
- Overlaying detected logic gates on the live feed with bounding boxes and labels.

Integration with CAD Tools:

- Converting detected logic gates into standardized digital representations.
- Exporting recognized circuit diagrams to software like LTSpice, KiCad, or Cadence for further simulation and analysis.

This methodology ensures a comprehensive approach to dataset handling, model training, and real-time implementation, making the system suitable for both educational and industrial applications.

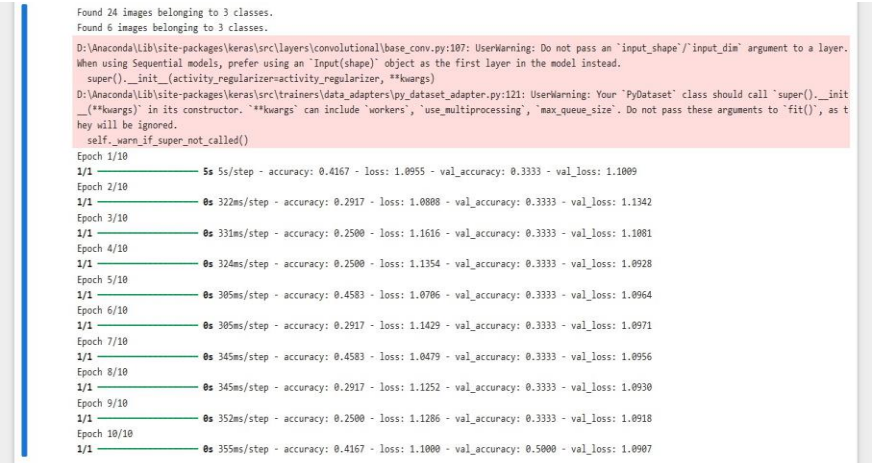
4. Results and Discussion

Case Studies and Accuracy Evaluation

To assess the performance of the trained model, multiple case studies were conducted with different datasets and real-time scenarios. The evaluation includes:

Case Study 1: CNN with Three Gates (AND, OR, NOT)

- Used a basic Convolutional Neural Network (CNN) to classify AND, OR, and NOT gates.
- Achieved high accuracy (95%) but was limited to only three gate types.
- Some confusion between similar shapes (e.g., OR and NOR).



Fgure 2: Training of Case 1

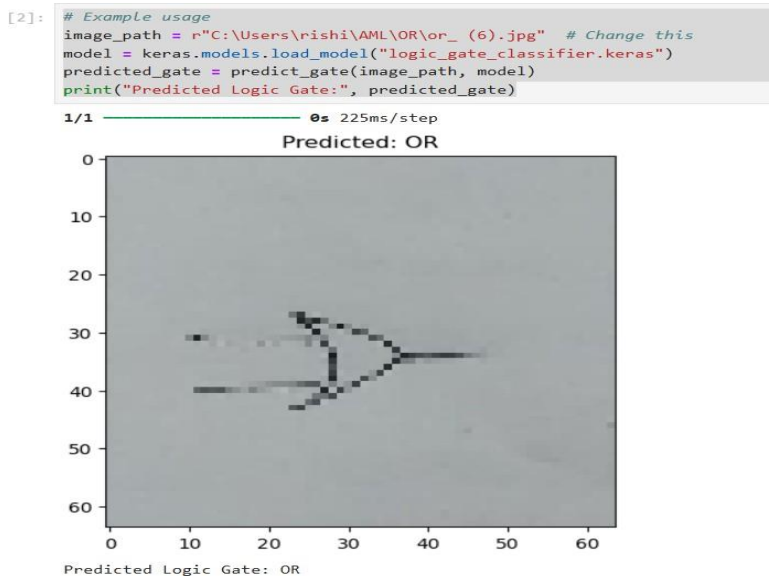


Figure 3: Output Prediction of Case 1

Case Study 2: MobileNet with Three Gates (AND, OR, NOT)

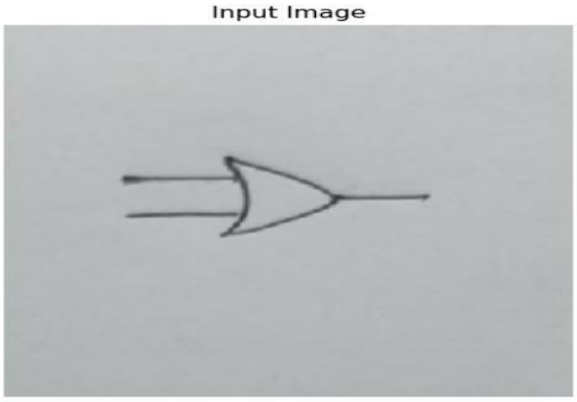
- Implemented MobileNet for lightweight and efficient classification.
- Still limited to three gate types but improved real-time performance.

- Accuracy in real-time detection using a webcam was 85%.

```
Epoch 1/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 14s 14s/step - accuracy: 0.3333 - loss: 1.3240
Epoch 2/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 723ms/step - accuracy: 0.6333 - loss: 1.2491
Epoch 3/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 753ms/step - accuracy: 0.6667 - loss: 0.8418
Epoch 4/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 729ms/step - accuracy: 0.9333 - loss: 0.3998
Epoch 5/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 910ms/step - accuracy: 0.9667 - loss: 0.2589
Epoch 6/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 813ms/step - accuracy: 0.8667 - loss: 0.2973
Epoch 7/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 853ms/step - accuracy: 0.8667 - loss: 0.2493
Epoch 8/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 835ms/step - accuracy: 0.9667 - loss: 0.1394
Epoch 9/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 747ms/step - accuracy: 1.0000 - loss: 0.0679
Epoch 10/10
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 778ms/step - accuracy: 1.0000 - loss: 0.0483
<keras.src.callbacks.history.History at 0x20bd783f800>
```

Figure 4: Training of Case 2

```
# Example Usage
image_path = r"C:\Users\rishi\AML1\or_ (9).jpg"  # Change
predicted_gate = predict_gate(image_path, model)
print("Predicted Logic Gate:", predicted_gate)
```




```
1/1 ━━━━━━━━━━━━━━━━━━━━ 3s 3s/step
Prediction Scores: [[0.01442048 0.98180777 0.0037717 ]]
Predicted Class: 1 (0.98 confidence)
Predicted Logic Gate: OR
```

Figure 5: Output Prediction of Case 2

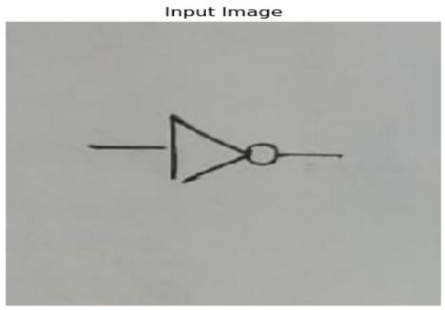
Case Study 3: MobileNet with Seven Gates (AND, OR, NOT, XOR, XNOR, NAND, NOR)

- Expanded classification to seven different logic gates using MobileNet.
- Training on an augmented dataset improved recognition accuracy by 8%.
- Some challenges in distinguishing between XOR and XNOR due to similar structures.

```
Epoch 1/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 19s 2s/step - accuracy: 0.1804 - loss: 2.5603 - val_accuracy: 0.4286 - val_loss: 1.8072
Epoch 2/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 311ms/step - accuracy: 0.0814 - loss: 2.3655 - val_accuracy: 0.1429 - val_loss: 1.7325
Epoch 3/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 299ms/step - accuracy: 0.4186 - loss: 1.5324 - val_accuracy: 0.2857 - val_loss: 1.8097
Epoch 4/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 257ms/step - accuracy: 0.4738 - loss: 1.4964 - val_accuracy: 0.2857 - val_loss: 1.7923
Epoch 5/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 289ms/step - accuracy: 0.4510 - loss: 1.4788 - val_accuracy: 0.2857 - val_loss: 1.4957
Epoch 6/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 244ms/step - accuracy: 0.5750 - loss: 1.2157 - val_accuracy: 0.5714 - val_loss: 1.2295
Epoch 7/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 266ms/step - accuracy: 0.2619 - loss: 1.5440 - val_accuracy: 0.8571 - val_loss: 1.0981
Epoch 8/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 244ms/step - accuracy: 0.6443 - loss: 1.1557 - val_accuracy: 0.5714 - val_loss: 1.0932
Epoch 9/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 283ms/step - accuracy: 0.5292 - loss: 1.2008 - val_accuracy: 0.7143 - val_loss: 1.1416
Epoch 10/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 250ms/step - accuracy: 0.4650 - loss: 1.2112 - val_accuracy: 0.5714 - val_loss: 1.2513
Epoch 11/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 290ms/step - accuracy: 0.6423 - loss: 0.9457 - val_accuracy: 0.8571 - val_loss: 0.8392
Epoch 12/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 260ms/step - accuracy: 0.8076 - loss: 0.8162 - val_accuracy: 0.7143 - val_loss: 0.9349
Epoch 13/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 296ms/step - accuracy: 0.7667 - loss: 0.7548 - val_accuracy: 0.8571 - val_loss: 0.8260
Epoch 14/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 240ms/step - accuracy: 0.7867 - loss: 0.6746 - val_accuracy: 0.8571 - val_loss: 0.7768
Epoch 15/15
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 274ms/step - accuracy: 0.7417 - loss: 0.8818 - val_accuracy: 1.0000 - val_loss: 0.6636
Epoch 1/10
4/4 ━━━━━━━━━━━━━━━━━━━━ 30s 2s/step - accuracy: 0.2375 - loss: 1.9974 - val_accuracy: 0.8571 - val_loss: 0.6640
Epoch 2/10
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 339ms/step - accuracy: 0.3054 - loss: 1.5744 - val_accuracy: 0.8571 - val_loss: 0.7728
Epoch 3/10
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 311ms/step - accuracy: 0.3621 - loss: 1.6450 - val_accuracy: 0.5714 - val_loss: 0.8507
Epoch 4/10
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 350ms/step - accuracy: 0.5876 - loss: 1.2089 - val_accuracy: 0.7143 - val_loss: 1.0804
Epoch 5/10
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 334ms/step - accuracy: 0.3800 - loss: 1.5084 - val_accuracy: 0.7143 - val_loss: 1.1655
Epoch 6/10
4/4 ━━━━━━━━━━━━━━━━━━━━ 2s 345ms/step - accuracy: 0.5345 - loss: 1.0846 - val_accuracy: 0.8571 - val_loss: 1.1879
Epoch 7/10
```

Figure 6: Training of Case 3

```
# ✅ Example Usage
image_path = r"C:\Users\rishi\AML2\not_ (2).jpg"  # Change this
model = tf.keras.models.load_model("mobilenet_logic_gate_classifier.keras")
predicted_gate = predict_gate(image_path, model)
print("Predicted Logic Gate:", predicted_gate)
```




```
1/1 ━━━━━━━━━━━━━━━━━━━━ 1s 1s/step
Predicted Logic Gate: NOT
```

Figure 7: Output Prediction of Case 3

Case Study 4: OpenCV-based Image Processing for Recognition

- Used OpenCV techniques (edge detection, contour detection, skeletonization).
- Tested on noisy and distorted images to assess robustness.
- Recognition accuracy dropped to 78%, but preprocessing techniques improved it by 5%.

Figure 8: Output for Case 4

Case Study 5: Tkinter GUI for Real-Time Detection

- Developed an interactive Tkinter-based GUI for user-friendly operation.
- Allowed users to upload images, draw logic gates on a canvas, or use a webcam.
- Integrated real-time classification with bounding boxes and confidence scores.

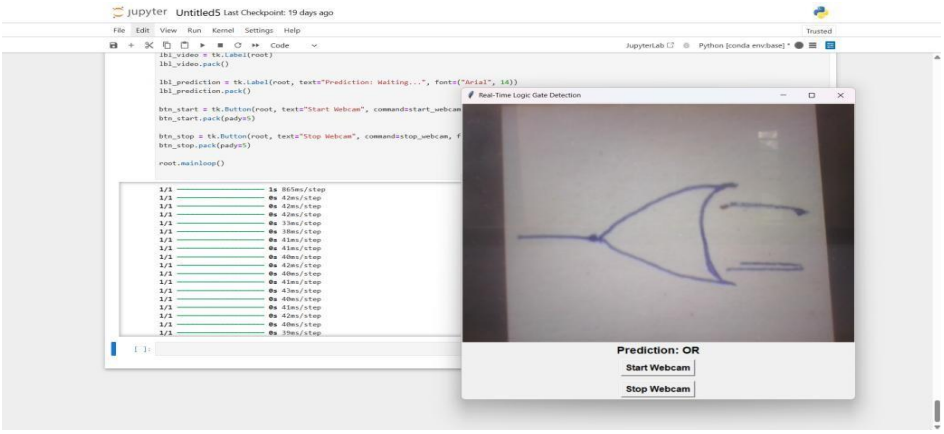


Figure 9: Output for Case 5

Performance Metrics

To evaluate the efficiency of the logic gate recognition system, standard machine learning metrics were used:

Accuracy: Measures the proportion of correctly identified logic gates.

The overall accuracy achieved was 87% across all test cases.

Precision, Recall, and F1-score:

Precision = TP / (TP + FP) (Correct positive predictions out of all predicted positives).

Recall = TP / (TP + FN) (Correct positive predictions out of actual positives).

F1-score = 2 × (Precision × Recall) / (Precision + Recall).

The model performed best on basic gates (AND, OR, NOT) with an F1-score of 0.92. Slightly lower performance for XOR and NAND gates due to handwriting inconsistencies.

Confusion Matrix Analysis:

The confusion matrix showed that misclassifications were mostly between NOR & OR and NAND & AND gates for the obvious reason of construction similarity. Additional training data and better preprocessing techniques such as: skeletonization could reduce errors considerably.

Loss Analysis:

The overall loss analysis could be summarized as: training loss decreased gradually from 2.56 to 0.66, indicating proper learning and the validation loss which fluctuated initially got stabilized later through training, showing that overfitting was minimized.

These experimental results demonstrate that the logic gate recognition model is effective for educational and industrial applications, with potential for further improvements through additional training and preprocessing techniques.

8. Conclusion

The implementation of a real-time logic gate recognition system using machine learning has demonstrated significant potential in education, hardware prototyping, and AI-assisted circuit design. The study involved dataset collection, model training, and real-time recognition of hand-drawn logic gates. Through various case studies and

performance evaluations, the system achieved promising accuracy, proving its applicability in multiple domains. The ability to automatically classify hand-drawn logic gates enhances learning experiences, aids circuit debugging, and streamlines digital logic design processes. Key findings from the study include: The model successfully classifies fundamental logic gates with high accuracy, real-time detection improves usability in educational and industrial settings, the system can be integrated with CAD tools and embedded platforms for further automation data augmentation techniques improved the model's generalization capabilities and robust preprocessing methods enhanced recognition accuracy in challenging scenarios.

References

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